In re Patent Application of:
GUINEA ET AL.
Serial No. **09/636,099**
Filing Date: **August 10, 2000**
_____/

In the Specification:

Please replace the paragraph beginning at page 4, line 20, with the following rewritten paragraph:

With reference to Figure 1, a circuit for detecting timing in a data flow BK comprises a circuit 1 for generating a local clock signal CK. The local clock signal CK is supplied to a circuit 2 to obtain, from the signal, four local timing signals Q1, Q2, Q3, Q4 having the same period T. This period is equal or substantially equal to the bit-time of the data flow BK. The signals Q1-Q4 are out of phase with one another by T/4. The signal Q2 is delayed by T/4 relative to the signal Q1. The signal Q3 is delayed by T/4 relative to the signal Q2, and by T/2 relative to the signal Q1. That is, the signal Q3 is in quadrature relative to the signal ~~Q1.~~ Q2. The signal Q4 is delayed by T/4 relative to the signal Q3.

Please replace the paragraph beginning at page 6, line 5, with the following rewritten paragraph:

The circuit of Figure 3 performs the logic function:

+/- = Q1' AND ~~Q2N',~~ Q2N' OR Q3' AND Q4N'

After the flip-flops have been loaded with the values applied to their inputs, Q1', Q2N', Q3', Q4N' are respectively equal to Q1, Q2N, Q3, Q4N.